

EAST SEARCH

11/18/05

L#	Hits	Search String	Databases
S1	8202	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S2	1108	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S3	417	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S4	2468	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S5	2206	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S6	918	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S7	299	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S8	54	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S9	311	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S10	59	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S11	74	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S12	90	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S13	1446	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S14	99	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S15	192	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S16	48	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S17	142	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S18	73	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S19	49	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S20	94	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S21	74	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S22	130	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S23	177	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S24	21	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S25	36	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S26	8	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S27	28	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S28	32	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S29	24	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S30	40	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S31	20	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S32	36	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S33	122	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S34	156	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S35	4	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S36	9	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S37	23	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S38	41	((digital or integraed) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S39 727 (((((digital or integrated) near2 circuit\$1) or logic) with simulat\$3) and ((("electromagnetic interf US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S40 270 (((((digital or integrated) near2 circuit\$1) or logic) with simulat\$3) and ((("electromagnetic interf US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

S41	7	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S42	63	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S43	4	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S44	93	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S45	4	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S46	26	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (waveform\$1 with (curre US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S47	94	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S48	10	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (waveform\$1 with rectan US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S49	0	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (waveform\$1 with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S50	3	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (waveform\$1 with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S51	0	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S52	75	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S53	31	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S54	16	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S55	0	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S56	22	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S57	27	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S58	12	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S59	8	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S60	122	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (((("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S61	727	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and ("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S62	746	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (((("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S63	145	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (((("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S64	2	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3) and (((("electromagnetic inter US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S65	13	6,237,126.pn. or "6,253,354".pn. or "5,835,380".pn. "5,617,325".pn. or "6,212,665".pn. or "6,3 US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S66	9387	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3
S67	1331	S66 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or noi US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S68	488	S66 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or no US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
S69	2511	S66 and ("gate level" or gate\$1 or cell\$1 or transistor\$1) with simulat\$3)
S70	368	S66 and (waveform\$1 with (current or voltage))
S71	3461	S67 or S68 or S69
S72	272	S70 and S71
S73	368	S70 or S72
S75	1	S74 and slew
S76	59	S73 and slew
S77	25	S76 and (output near2 slew)
S78	48	S72 and slew
S79	14	S78 and (output near2 slew)
S74	17	S73 and (triangular near2 waveform)
S80	16	S72 and (triangular near2 waveform)
S81	53	S70 and (waveform\$1 near2 (rectangular or triangular or exponential or function))
S82	3	S77 and S81
S83	15	S81 and slew
L13	9387	(((digital or integraed) near2 circuit\$1) or logic) with simulat\$3
L14	1331	L13 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or noi US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L15	488	L13 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or noi US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

L16	2511	L13 and ("gate level" or gate\$1 or cell\$1 or transistor\$1) with simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L17	368	L13 and (waveform\$1 with (current or voltage))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L18	3461	L14 or L15 or L16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L19	272	L17 and L18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L20	368	L17 or L19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L21	59	L20 and slew	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L22	25	L21 and (output near2 slew)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L23	53	L17 and (waveform\$1 near2 (rectangular or triangular or exponential or function))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L24	3	L22 and L23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L25	351	L13 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or noi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L26	5	25 and (triangular.CLM.)	US-PGPUB
L27	3	25 and (slew.CLM.)	US-PGPUB
L1	8	6,876,210.pn. or "6,782,347".pn. or "6,810,340".pn. or "6,754,598".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L2	0	1 and ("triangular waveform")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L3	0	1 and ("output slew")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

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Hidetoshi Narahara

EAST SEARCH

11/18/05

Results of search set L36:([The compound statement])

Document Kind	Codes	Title	Issue Date	Current OR	Abstract
US	20040117169	A1 Method and system for short-circuit current modeling in CMOS integrated circuits	20040617	703/15	
US	20040103381	A1 Semiconductor integrated circuit designing apparatus, semiconductor integrated circuit design	20040527	716/5	
US	20040073880	A1 Method and system for designing circuit layout	20040415	716/8	
US	20040044510	A1 Fast simulation of circuitry having sol transistors	20040304	703/14	
US	20040034840	A1 Method for analysis of interconnect coupling in VLSI circuits	20040219	716/6	
US	20030212843	A1 Method and apparatus for selectively providing data pre-emphasis based upon data content	20031113	710/100	
US	20030208725	A1 Method of designing semiconductor integrated circuit device and semiconductor integrated ci	20031106	716/1	
US	20030204818	A1 Method for creating a characterized digital library for a digital circuit design	20031030	716/1	
US	20030204817	A1 Method for creating a characterized digital library for a digital circuit design	20031030	716/1	
US	20030145296	A1 Formal automated methodology for optimal signal integrity characterization of cell libraries	20030731	716/6	
US	20030115568	A1 Method of designing, fabricating, testing and interconnecting an IC to external circuit nodes	20030619	716/15	
US	20030115563	A1 Method for estimating peak crosstalk noise	20030619	716/5	
US	20030079191	A1 Cell-based noise characterization and evaluation	20030424	716/4	
US	20030074178	A1 Emulation system with time-multiplexed interconnect	20030417	703/25	
US	20030016044	A1 Method for analyzing failure of semiconductor integrated circuit and failure	20030123	324/765	
US	20020177990	A1 Distributed logic analyzer for use in a hardware logic emulation system	20021128	703/28	
US	20020174409	A1 System and method for analyzing power distribution using static timing analysis	20021121	716/6	
US	20020161568	A1 Memory circuit for use in hardware emulation system	20021031	703/25	
US	20020157069	A1 Method and apparatus for preparing a simulation model semiconductor integrated circuit at pr	20021024	716/5	
US	20020147555	A1 Method and apparatus for analyzing a source current waveform in a semiconductor integrat	20021010	702/70	
US	20020065643	A1 Method for optimizing electromagnetic interference and method for analyzing the electromag	20020530	703/19	
US	20020045995	A1 Electromagnetic interference analysis method and apparatus	20020418	702/77	

US 20020043667 A1	Method of designing semiconductor integrated circuit device and semiconductor integrated ci	20020418 257/202
US 20020035708 A1	Method and apparatus for generating test patterns used in testing semiconductor integrated c	20020321 714/25
US 20020024064 A1	Method of designing semiconductor integrated circuit device and semiconductor integrated ci	20020228 257/207
US 20020022951 A1	Method, apparatus and computer program product for determination of noise in mixed signal	20020221 703/16
US 20020011885 A1	Power model for EMI simulation to semiconductor integrated circuit , method of designing the	20020131 327/158
US 20020011827 A1	Fault simulation method and fault simulator for semiconductor integrated circuit	20020131 324/71.5
US 20010054917 A1	Driver circuit, receiver circuit, and semiconductor integrated circuit device	20011227 327/108
US 20010054174 A1	Programmable logic controller method, system and apparatus	20011220 714/4
US 20010043450 A1	System and method for servo control of nonlinear electromagnetic actuators	20011122 361/160
US 20010039649 A1	Programmable logic controller method, system and apparatus	20011108 717/128
US 20010037491 A1	Programmable logic controller method, system and apparatus	20011101 717/128
US 20010032329 A1	Storage media being readable by a computer, and a method for designing a semiconductor ir	20011018 716/6
US 20010029600 A1	Storage media being readable by a computer, and a method for designing a semiconductor ir	20011011 716/17
US 20010005898 A1	Timing verifying system in which waveform slew is considered	20010628 714/815
US 20010000427 A1	Method of incorporating interconnect systems into an integrated circuit process flow	20010426 333/33
US 6751579 B1	Method of scaling table based cell library timing models in order to take into account process.	20040615 703/2
US 6734704 B1	Voltage level-shifting control circuit for electronic switch	20040511 326/63
US 6732339 B2	Cell-based noise characterization and evaluation	20040504 716/4
US 6732068 B2	Memory circuit for use in hardware emulation system	20040504 703/24
US 6694464 B1	Method and apparatus for dynamically testing electrical interconnect	20040504 714/725
US 6691284 B2	Method for creating a characterized digital library for a digital circuit design	20040217 716/1
US 6687205 B1	Parallel coded spread spectrum communication for data storage	20040203 369/47.19
US 6668333 B1	Method and apparatus for evaluating effects of switching noise in digital and analog circuitry	20031223 713/500
US 6634015 B2	Computer-readable storage media stored with a delay library for designing a semiconductor ii	20031014 716/6
US 6629299 B1	Delay library representation method, delay library generation method and delay calculation m	20030930 716/6
US 6629289 B2	Timing verifying system in which waveform slew is considered	20030930 714/815
US 6615394 B2	Method and apparatus for preparing a simulation model for semiconductor integrated circuit e	20030902 716/5
US 6611943 B2	Method of designing semiconductor integrated circuit device and semiconductor integrated ci	20030826 716/1
US 6604066 B1	Method and apparatus for calculating delay for logic circuit and method of calculating delay d:	20030805 703/19
US 6574743 B1	Programmable logic controller method, system and apparatus	20030603 713/502
US 6542443 B1	Efficient linearization of saturation channels	20030401 369/13.02
US 6542011 B2	Driver circuit, receiver circuit, and semiconductor integrated circuit device	20030401 327/108
US 6539531 B2	Method of designing, fabricating, testing and interconnecting an IC to external circuit nodes	20030325 716/15
US 6498583 B1	Real time multiple simulated targets generator for mono pulse radar	20021224 342/169
US 6493853 B1	Cell-based noise characterization and evaluation	20021210 716/5
US 6462978 B2	Method of designing semiconductor integrated circuit device and semiconductor integrated ci	20021008 365/63
US 6461882 B2	Fault simulation method and fault simulator for semiconductor integrated circuit	20021008 438/17
US 6415181 B1	Implantable medical device incorporating adiabatic clock-powered logic	20020702 607/16
US 6393385 B1	Knowledge driven simulation time and data reduction technique	20020521 703/15
US 6377912 B1	Emulation system with time-multiplexed interconnect	20020423 703/28
US 6370678 B1	System and method for adjusting logic synthesis based on power supply circuit models	20020409 716/18
US 6370072 B1	Low voltage single-input DRAM current-sensing amplifier	20020409 365/210
US 6367061 B1	Semiconductor integrated circuit and manufacturing method therefor, semiconductor macro c	20020402 716/10
US 6340825 B1	Method of designing semiconductor integrated circuit device and semiconductor integrated ci	20020122 257/207
US 6304998 B1	Method of manufacturing integrated circuit device	20011016 716/4
US 6298466 B1	Method and system for synthesizing operational amplifiers for amplifying systems with minim.	20011002 716/1
US 6278964 B1	Hot carrier effect simulation for integrated circuits	20010821 703/19

US 6253354 B1	Method and apparatus for analyzing variations in source voltage of semiconductor device	20010626 716/4
US 6242951 B1	Adiabatic charging logic circuit	20010605 326/98
US 6208594 B1	Efficient linearization of saturation channels	20010327 369/13.02
US 6208497 B1	System and method for servo control of nonlinear electromagnetic actuators	20010327 361/160
US 6160382 A	Method and apparatus for determining Characteristic parameters of a charge storage device	20001212 320/136
US 6125334 A	Module-configurable full-chip power profiler	20000926 702/60
US 6066177 A	Method and apparatus for calculating delay for logic circuit and method of calculating delay d:	20000523 703/19
US 6047247 A	Method of estimating degradation with consideration of hot carrier effects	20000404 702/117
US 6000829 A	Semiconductor integrated circuit capable of compensating for fluctuations in power supply vol	19991214 700/95
US 5960191 A	Emulation system with time-multiplexed interconnect	19990928 703/28
US 5943490 A	Distributed logic analyzer for use in a hardware logic emulation system	19990824 703/28
US 5880616 A	Digital logic level conversion circuit with a small sinusoidal wave input	19990309 327/333
US 5872531 A	Signal encoder/decode system	19990216 341/110
US 5864311 A	Systems for enhancing frequency bandwidth	19990126 341/155
US 5857164 A	System for calculating current consumption characteristics of cells	19990105 702/64
US 5854600 A	Hidden side code channels	19981229 341/155
US 5852445 A	Method of verifying integrated circuit operation by comparing stored data structures correspo	19981222 345/440
US 5838947 A	Modeling, characterization and simulation of integrated circuit power behavior	19981117 703/14
US 5838274 A	Systems for achieving enhanced amplitude resolution	19981117 341/155
US 5835380 A	Simulation based extractor of expected waveforms for gate-level power analysis tool	19981110 716/2
US 5808574 A	Systems for achieving enhanced frequency resolution	19980915 341/110
US 5768145 A	Parametrized waveform processor for gate-level power analysis tool	19980616 703/14
US 5712589 A	Apparatus and method for performing adaptive power regulation for an integrated circuit	19980127 327/538
US 5692907 A	Interactive cardiac rhythm simulator	19971202 434/262
US 5675523 A	Waveform data generating apparatus	19971007 708/8
US 5640161 A	Silent data conversion system with sampling during electrical silence	19970617 341/122
US 5638074 A	Method and apparatus for slew limiting	19970610 341/155
US 5617325 A	Method for estimating interconnect delays in integrated circuits	19970401 716/6
US 5608518 A	Test method for predicting hot-carrier induced leakage over time in short-channel IGFETS an	19970225 703/13
US 5600578 A	Test method for predicting hot-carrier induced leakage over time in short-channel IGFETS an	19970204 703/14
US 5568395 A	Modeling and estimating crosstalk noise and detecting false logic	19961022 716/4
US 5553008 A	Transistor-level timing and simulator and power analyzer	19960903 703/14
US 5541529 A	Field programmable gate array transferring signals at high speed	19960730 326/39
US 5481484 A	Mixed mode simulation method and simulator	19960102 703/14
US 5479168 A	Compatible signal encoder/decode system	19951226 341/110
US 5459673 A	Method and apparatus for optimizing electronic circuits	19951017 716/6
US 5452225 A	Method for defining and using a timing model for an electronic circuit	19950919 703/19
US 5446676 A	Transistor-level timing and power simulator and power analyzer	19950829 703/19
US 5396527 A	Recovered energy logic circuits	19950307 377/57
US 5384720 A	Logic circuit simulator and logic simulation method having reduced number of simulation eve	19950124 703/16
US 5317207 A	Integrated circuit having reduced electromagnetic emissions an integrated circuit including a '	19940531 326/26
US 5298851 A	Multiple application voltage regulator system and method	19940329 322/28
US 5223775 A	Apparatus and related method to compensate for torque ripple in a permanent magnet electri	19930629 318/432
US 5148514 A	Neural network integrated circuit device having self-organizing function	19920915 706/34
US 5115386 A	Circuit for controlling an electric power supply apparatus, a method therefor and an uninterru	19920519 363/41
US 5036479 A	Modular automated avionics test system	19910730 702/121
US 4516039 A	Logic circuit utilizing a current switch circuit having a non-threshold transfer characteristic	19850507 326/18

US 4459457 A	Feedback welder control system	19840710 219/110
US 4459456 A	Feedback welder control system	19840710 219/110
US 4394776 A	Priority channel system for a synthesized transceiver	19830719 455/76
US 4303921 A	Digital readout PRF measuring device	19811201 342/13
US 3826899 A	BIOLOGICAL CELL ANALYZING SYSTEM	19740730 377/10
US 3699336 A	BIOLOGICAL CELL ANALYZING SYSTEM	19721017 250/461.2

Results of search set L22:

Document Kind	Codes Title	Issue Date	Current OR	Abstract
US 20050117510 A1	Cell Current ReConstruction Based on Cell Delay and Node Slew Rate	20050602	370/229	
US 20030105620 A1	System, method and article of manufacture for interface constructs in a programming language	20030605	703/22	
US 20030074177 A1	System, method and article of manufacture for a simulator plug-in for co-simulation purposes	20030417	703/22	
US 20030046671 A1	System, method and article of manufacture for signal constructs in a programming language	20030306	717/141	
US 20030046668 A1	System, method and article of manufacture for distributing IP cores	20030306	717/131	
US 20030037321 A1	System, method and article of manufacture for extensions in a programming language capab	20030220	717/149	
US 20030033594 A1	System, method and article of manufacture for parameterized expression libraries	20030213	717/141	
US 20030033588 A1	System, method and article of manufacture for using a library map to create and maintain IP	20030213	717/107	
US 20030028864 A1	System, method and article of manufacture for successive compilations using incomplete par	20030206	717/141	
US 20020199173 A1	System, method and article of manufacture for a debugger capable of operating across multi	20021226	717/129	
US 20020174409 A1	System and method for analyzing power distribution using static timing analysis	20021121	716/6	
US 6959250 B1	Method of analyzing electromagnetic interference	20051025	702/75	
US 6851095 B1	Method of incremental recharacterization to estimate performance of integrated designs	20050201	716/4	
US 6832361 B2	System and method for analyzing power distribution using static timing analysis	20041214	716/6	
US 6832182 B1	Circuit simulator	20041214	703/13	
US 6691301 B2	System, method and article of manufacture for signal constructs in a programming language	20040210	717/114	
US 6499129 B1	Method of estimating performance of integrated circuit designs	20021224	716/4	
US 6278964 B1	Hot carrier effect simulation for integrated circuits	20010821	703/19	
US 6047247 A	Method of estimating degradation with consideration of hot carrier effects	20000404	702/117	
US 5959481 A	Bus driver circuit including a slew rate indicator circuit having a one shot circuit	19990928	327/170	
US 5852445 A	Method of verifying integrated circuit operation by comparing stored data structures correspo	19981222	345/440	
US 5841672 A	Method and apparatus for verifying signal timing of electrical circuits	19981124	716/6	
US 5838947 A	Modeling, characterization and simulation of integrated circuit power behavior	19981117	703/14	
US 5473548 A	Apparatus for computing power consumption of MOS transistor logic function block	19951205	716/6	
US 4211065 A	Automatic system for setting digital watches	19800708	368/47	

Interference checking

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Databases

L#	Hits	Search String	Databases
L13	9387	((digital or integrated) near2 circuit\$1) or logic) with simulat\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L14	1331	L13 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or not)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L15	488	L13 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or not)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L16	2511	L13 and ("gate level" or gate\$1 or cell\$1 or transistor\$1) with simulat\$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L17	368	L13 and (waveform\$1 with (current or voltage))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L18	3461	L14 or L15 or L16	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L19	272	L17 and L18	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L20	368	L17 or L19	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L21	59	L20 and slew	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L22	25	L21 and (output near2 slew)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L23	53	L17 and (waveform\$1 near2 (rectangular or triangular or exponential or function))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L24	3	L22 and L23	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L25	351	L13 and ("electromagnetic interference" or EMI or (electromagnetic near2 emission\$1) or not)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
L26	5	25 and (triangular.CLM.)	US-PGPUB
L27	3	25 and (slew.CLM.)	US-PGPUB

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US	20030046668 A1	System, method and article of manufacture for distributing IP cores	20030306	717/131	
US	20030037321 A1	System, method and article of manufacture for extensions in a programming language capable	20030220	717/149	
US	20030033594 A1	System, method and article of manufacture for parameterized expression libraries	20030213	717/141	
US	20030033588 A1	System, method and article of manufacture for using a library map to create and maintain IP	20030213	717/107	
US	20030028864 A1	System, method and article of manufacture for successive compilations using incomplete par	20030206	717/141	
US	20020199173 A1	System, method and article of manufacture for a debugger capable of operating across multi	20021226	717/129	
US	20020174409 A1	System and method for analyzing power distribution using static timing analysis	20021121	716/6	
US	6959250 B1	Method of analyzing electromagnetic interference	20051025	702/75	
US	6851095 B1	Method of incremental recharacterization to estimate performance of integrated designs	20050201	716/4	
US	6832361 B2	System and method for analyzing power distribution using static timing analysis	20041214	716/6	

US 6832182 B1	Circuit simulator	20041214 703/13
US 6691301 B2	System, method and article of manufacture for signal constructs in a programming language	20040210 717/114
US 6499129 B1	Method of estimating performance of integrated circuit designs	20021224 716/4
US 6278964 B1	Hot carrier effect simulation for integrated circuits	20010821 703/19
US 6047247 A	Method of estimating degradation with consideration of hot carrier effects	20000404 702/117
US 5959481 A	Bus driver circuit including a slew rate indicator circuit having a one shot circuit	19990928 327/170
US 5852445 A	Method of verifying integrated circuit operation by comparing stored data structures correspond	19981222 345/440
US 5841672 A	Method and apparatus for verifying signal timing of electrical circuits	19981124 716/6
US 5838947 A	Modeling, characterization and simulation of integrated circuit power behavior	19981117 703/14
US 5473548 A	Apparatus for computing power consumption of MOS transistor logic function block	19951205 716/6
US 4211065 A	Automatic system for setting digital watches	19800708 368/47